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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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| **APPLICANT:** | Utz Wever, et al. | **ATTORNEY DOCKET NO.** | P99,0886 |
| **SERIAL NO.** | 09/308,478 | **GROUP ART UNIT:** | 2774 |
| **FILING DATE:** | May 17, 1999 | **EXAMINER:** | |
| **INVENTION:** | "COMPUTER ASSISTED METHOD FOR PARTITIONING AN ELECTRICAL CIRCUIT" | | |

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INFORMATION DISCLOSURE STATEMENT TRANSMITTAL LETTER

**HON. ASSISTANT COMMISSIONER OF PATENTS**
**Washington, D.C. 20231**

Sir:

Submitted herewith is an Information Disclosure Statement for consideration in the above-identified application. This Information Disclosure Statement is submitted:

☒ Within 3 months (1) of filing date of a national application; (2) of date of entry of the national stage as set forth in 37 C.F.R. §1.491 in an international application; or (3) before the mailing date of a first Office Action on the merits, whichever occurs last. (No fee is required.)

☐ After the mailing date of a first Office Action but before (1) mailing of a final action under 37 C.F.R. §1.113; or (2) mailing of a notice of allowance under §1.311, whichever occurs first.

- ☐ Payment for the fee set forth in 37 C.F.R. §1.17(p) accompanies this submission; or
- ☐ The certification specified in 37 C.F.R. §1.97(e) is made below. (No fee is required.)

☐ After the mailing of (1) a final action under 37 C.F.R. §1.113; or (2) a notice of allowance under 37 C.F.R. §1.311 whichever occurs first, but **before** payment of the issue fee. The certification specified in 37 C.F.R. §1.97(e) is made below. The Commissioner hereby is petitioned to consider the Information Disclosure Statement accompanying this submission. Payment for the Petition fee set forth in 37 C.F.R. §1.17(i)(1) accompanies this submission.

☐ The undersigned counsel for applicant(s) hereby certifies each item of information identified in the Information Disclosure Statement was cited in a communication from a foreign Patent Office in a counterpart foreign application not more than three months prior to the filing of this Information Disclosure Statement.

☐ The undersigned counsel for applicant(s) hereby certifies that no item of information contained in the Information Disclosure Statement was cited in a communication from a foreign Patent Office in a counterpart foreign application, or to the knowledge of the undersigned, after making reasonable inquiry, was known to any individual designated in 37 C.F.R. §1.56(c) more than three months prior to the filing of this Information Disclosure Statement.

☐ A check in the amount of $____ to cover any required fee is enclosed.

☒ The Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Account No. 08-2290. *A duplicate copy of this sheet is enclosed for this purpose.*

Very respectfully,

HILL, STEADMAN & SIMPSON
A Professional Corporation

By _____ Reg. 32,919

When phoning re this application,
please call (312) 876-0200 Ext. 3084

Hill, Steadman & Simpson, P.C.
Sears Tower, 85th Floor
Chicago, Illinois 60606
Telephone (312) 876-0200

CERTIFICATE OF MAILING

I hereby certify that this Information Disclosure Statement is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to the Commissioner of Patents and Trademarks, Washington D.C. on September 28, 1999 .

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INFORMATION DISCLOSURE STATEMENT

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SEP 30 1999
PATENT & TRADEMARK OFFICE

Hon. Assistant Commissioner of Patents
Washington, D.C. 20231

S I R:

## I. INTRODUCTION

In accordance with the provisions of 37 C.F.R. Section 1.56, applicant requests that citation and examination of the documents identified on the attached form PTO 1449 be made during the course of the prosecution of the above-identified patent application. A copy of each of these documents is enclosed for the convenience of the examiner.

## II. DOCUMENTS

OTHER ITEMS OF INFORMATION

AT I. Hoefer, et al., *SPICE Analyseprogramm fur elektronische Schaltungen*, Springer, Berlin (1985), pp. 7-22

AU U. Kleis, et al., *Domain Decomposition Methods for Circuit Simulation*, Proceedings of the 8th Workshop on Parallel and Distributed Simulation, PADS, Edinburgh, UK (July, 1994), pp. 183-86

AV U. Wever, et al. *Parallel Transient Analysis for Circuit Simulation*, Proceedings of the 29th Annual Hawaii International Conference on System Sciences (1946), pp. 442-47

AW B. Riess, et al., *Partitioning Very Large Circuits Using Analytical Placement Techniques*, Proceedings of the 31st ACM/IEEE Design Automation Conference (1994), pp. 646-51

AX P. Johannes, *Partitioning of VLSI Circuits and Systems*, 33rd Design and Automation Conference, Las Vegas (June 3-7, 1996), pp. 83-87

BT J. Cong, et al., *A Parallel Bottom-up Clustering Algorithm with Applications to Circuit Partitioning in VLSI Design*, In: 30th Design Automation Conference, June 14-18, 1993, pp. 755-760

BU J. Li, et al., *New Spectral Linear Placement and Clustering Approach*, 33rd Design Automation Conference, Las Vegas (June 3-7, 1996), pp. 88-93

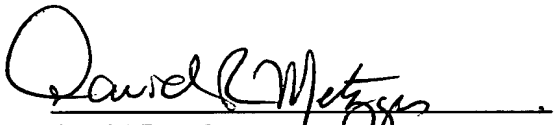
BV T. Kage, et al., *A Circuit Partitioning Approach for Parallel Circuit Simulation*, IEICE Trans Fundamentals, Vol. E77-A, No. 31 (1993), pp. 461-65

BW G. Hung, et al., *Improving the Performance of Parallel Relaxation-Based Circuit Simulators*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, New York (November 12, 1993), No. 11, pp. 1762-74

## III. REMARKS

The above identified documents, Items AT, AU, AV, AW, AX and BT are referred to in the application and incorporated by reference therein. Items BU, BV and BW contain relevant subject matter.

Respectfully submitted,



Reg. 32,919

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